Unipolar Devices
<table>
<thead>
<tr>
<th>Term (Index)</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>unipolar device</td>
<td>semiconductor device (\rightarrow) operation is based predominantly on the use of majority charge carriers e.g. all transistors based on the field effect fall into this category; alternative to bipolar device.</td>
</tr>
<tr>
<td>bipolar device</td>
<td>semiconductor device (\rightarrow) operation is based on the use of both majority and minority charge carriers; all p-n junction based devices fall into this category; alternative to unipolar device.</td>
</tr>
</tbody>
</table>

**FET**: Field Effect Transistor

**JFET**: Junction FET [Field Effect Transistor]

uses a reverse biased p-n junction to separate the gate from the body

**MOSFET**: Metal-Oxide-Semiconductor (MOS) Field Effect Transistor (FET)

(utilizes an insulator (typically \(\text{SiO}_2\)) between the gate and the body

**MESFET**: Metal-Semiconductor Field Effect Transistor (FET)

substitutes the p-n junction of the JFET with a Schottky barrier; used in GaAs and other III-V semiconductor materials.

**HEXFET** (Hexagon shaped), T (Trench) MOS, D (Double diffuse)MOS, U (Ultra Low Resistance) MOS, V (V-Groove) MOS,

**ZMOS**: Additional names which define the internal structure, not type
Historical context of FET development? The vacuum tube triode:
The Lilienfeld Story:

"It was in 1930 when the field-effect principle was first disclosed in a U.S. patent by Julius Lilienfeld, a former professor of physics at the University of Leipzig who immigrated to the United States."

"On December 16, 1947, the point-contact transistor was demonstrated by Walter H. Brattain and John Bardeen (Shockley 1972 & 1976), with William Shockley as an intensely interested observer. After an additional week of further experimentation and polishing of the demonstration, it was repeated for several times in key Bell Laboratories on December 23, 1947, the date that has come to be taken as the "official" date of bring it to practice. Walter H. Brattain, John Bardeen and William Shockley shared a Nobel prize for the transistor in 1956.

"The invention of the bipolar junction transistor in 1948 was the beginning of semiconductor electronics. This device and semiconductor diodes spawned a revolution in electronics. Drastic reduction in size, cost, and power consumption were achieved simultaneously with greatly increased equipment complexity and capability.

"At the same time, in 1948, Shockley and Pearson tried fabricating a simple FET using evaporated layers of germanium on dielectric. However, it was not until Bardeen has given theory on the surface state phenomenon and Shockley published his theoretical analysis of the unipolar field-effect transistor ....."
FET Generalities

- Every FET has at least three connections:
  - source (S)
    - akin to emitter (E) on BJT
  - drain (D)
    - akin to collector (C) on BJT
  - gate (G)
    - akin to base (B) on BJT
- Some have a body connection too
  - though often tied to source

Note:
All FETs except J-FETs have four terminals, which are known as the gate, drain, source and body/base/bulk. Compare these to the terms used for BJTs: base, collector and emitter. BJTs and J-FETs have no body terminal.
The Junction Field Effect Transistor (JFET)
FET Types

- Two flavors: n and p
- Two types: JFET, MOSFET
- MOSFETs more common
- JFETs conduct “by default”
  - when $V_{\text{gate}} = V_{\text{source}}$
- MOSFETs are “open” by default
  - must turn on deliberately
- JFETs have a p-n junction at the gate, so must not forward bias more than 0.6 V
- MOSFETs have total isolation: do what you want
MOSFET Switches

- MOSFETs, as applied to logic designs, act as **voltage-controlled switches**
  - **n-channel** MOSFET is closed (conducts) when positive voltage (+5 V) is applied, open when zero voltage
  - **p-channel** MOSFET is open when positive voltage (+5 V) is applied, closed (conducts) when zero voltage
- (MOSFET means metal-oxide semiconductor field effect transistor)
The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

Two Schematic Representations of a MOSFET
Junction Field Effect Transistors (JFETs)

More Realistic IC JFET Transistor
pinch-off: (Pinch off voltage is defined as minimum ground to source voltage for which drain current will become zero. If we apply this voltage between drain and source then at this potential drain current starts saturating.)
1. The termination of drain-source current flow in a field effect transistor.
2. The gate-source voltage at which a FET's channel is fully depleted and electrical current between drain and source is prevented.
3. That value of reverse bias voltage applied to the input of a J-FET linear amplifier to cut off its channel and reduce its output current to zero.
4. The gate-source voltage required to stop drain-source current flow in a field effect transistor.
Series 1: Operation at constant gate voltage
Series 2: Operation at constant drain-source voltage
Series 3: Operation at constant drain-source voltage
Note how the "metal" type influences the band structure under various bias conditions. In particular note that inversion is possible in the equilibrium state (zero gate-source voltage) and that the threshold voltage may be either positive or negative.

<table>
<thead>
<tr>
<th>Condition</th>
<th>&quot;Metal&quot; = p+ poly silicon</th>
<th>&quot;Metal&quot; = n+ poly silicon</th>
<th>&quot;Metal&quot; = aluminum</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Equilibrium</strong></td>
<td><img src="image" alt="Equilibrium Diagram" /></td>
<td><img src="image" alt="Equilibrium Diagram" /></td>
<td><img src="image" alt="Equilibrium Diagram" /></td>
</tr>
<tr>
<td>( V_G = 0 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Flat-band</strong></td>
<td><img src="image" alt="Flat-band Diagram" /></td>
<td><img src="image" alt="Flat-band Diagram" /></td>
<td><img src="image" alt="Flat-band Diagram" /></td>
</tr>
<tr>
<td>( V_G = V_{FB} = \phi_M - \phi_S )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Threshold</strong></td>
<td><img src="image" alt="Threshold Diagram" /></td>
<td><img src="image" alt="Threshold Diagram" /></td>
<td><img src="image" alt="Threshold Diagram" /></td>
</tr>
<tr>
<td>( V_G = V_T )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The Field Effect Transistor

The Field Effect Transistor (FET) is a 3-terminal device that has similar applications as the bipolar junction transistor. The main difference between the FET and the BJT is:

- **BJTs are current-controlled devices**
- **FETs are voltage controlled devices**

That is, in BJTs, the output current is dependent on the input base current, \( I_B \). In FETs, the output current is dependent of the input gate voltage (\( V_{GS} \)).

The two major types of FETs are **n-channel** and **p-channel**. BJTs are **bi-polar** devices by nature of its conduction levels being functions of two different charge carriers (electrons and holes), and FETs are **uni-polar** devices since they depend solely of only one charge carrier (electrons for n-channel and holes for p-channel).

FETs have much higher input impedances than BJT, but their ac voltage gains are usually less. FETs have better temperature stability and are smaller, making them more useful for IC designs.

In this section, we will be looking at 3 main types of FETs namely: Junction FET (JFET), Metal Oxide Semiconductor FET (MOSFET), and metal semiconductor FET.
The Field Effect Transistor

Structure and Characteristics of the JFET

The basic structure of the n-channel JFET consists of a n-channel between embedded layers of p-type material. The two layers of p-type material are connected together to form the Gate. The ends of the n-channel form the Drain and the Source of the JFET. As shown, two pn junctions are created. In the absence of biasing, depletion regions are formed at both junctions.

Whenever bias voltages are applied across the Drain and Source, but not to the Gate, a distinct flattening of the characteristic curves occurs. As $V_{DS}$ increases, the depletion region widens causing channel width to be reduced. This increases the resistance of the Channel until the condition known as Pinch-off occurs, labeled $V_P$ on the plot. When this happens, the JFET is saturated and $I_{DS}$ remains constant irrespective of further increase in $V_{DS}$. In this state, the JFET is an ideal current source.

In FETs: \[ I_D = I_S \] always
The Field Effect Transistor

Applying a Gate Voltage

If $V_{GS}$ is varied from 0V to $-V_P$, the following characteristic curves are obtained.

$V_{GS}$ gets more negative, it takes a lower $V_{DS}$ to reach saturation. When $V_{GS} = -V_P$, the device will essentially be in saturation with $I_D = 0$ mA. Note that in the Ohmic region, the JFET is operating as a voltage controlled resistor.

$$r_0 = \text{resistance when } V_{GS} = 0$$

$R_d$ is resistance at $V_{GS} \neq 0$

For n-channel JFET, typically

$r_0 = 10k$ ($V_{GS} = 0$, $V_P = -6V$) and $r_d = 40k\Omega$ at $V_{GS} = -3V$
The Field Effect Transistor

**p-Channel JFET**

The p-channel device is constructed in the same exact manner as the n-channel, but with the n and p-type regions reversed. For this curve, at pinch-off, $I_{DSS} = 6\text{mA}$ and when $V_{GS} = +6\text{V}$. 

![Diagram of p-channel JFET with circuit symbols and VDS vs. IDS curves]
The Field Effect Transistor

Transfer Characteristics

The relationship between $I_D$ and $V_{GS}$ is defined by Shockley’s equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where $I_{DSS}$ and $V_P$ are constants and $V_{GS}$ is variable and controllable.

The transfer function curve may be plotted from the characteristic curve, as shown. Notice the parabolic shape due to the square term relationship between $I_D$ and $V_{GS}$.

Remember that, when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $V_{GS} = V_P$, $I_D = 0 \text{ mA}$.
The Field Effect Transistor

MOSFET

Depending on the mode of operation, MOSFETs are categorized as either depletion type or enhancement type.

Depletion-type MOSFET: Basic Structure and Circuit Symbols

The basic structure of the n-channel Depletion type MOSFET is shown below. Notice that the Drain, Source and its connecting n-channel are embedded into a slab of p-type material. The substrate, SS is usually connected to the source terminal. The insulating layer of SiO2 prevents any kind of electrical contact of gate and channel. This gives the MOSFET its desirable feature of very high input impedance. This oxide layer forms a capacitor, $C_{ox}$, between gate and substrate.

Circuit symbols
The Field Effect Transistor

Basic Operation and Characteristics of the n-channel Depletion type MOSFET

As \( V_{GS} \) gets more negative, electrons in the channel or repelled into the p-type substrate where they will recombine with the holes there. This reduces the number of free electrons in the channel until \( I_D = 0 \). On the other hand, a +ve charge on the gate will draw electrons from the substrate into the channel, effectively increasing the amount of charge carriers, thus increasing \( I_D \).
The Field Effect Transistor

The Field Effect Transistor is a unipolar device that operates on a different principle from bipolar transistors. It consists of a semiconductor region with a channel, gate, source, and drain terminals.

(a) The schematic diagram of a p-channel depletion-type MOSFET shows the channel between the source (S) and drain (D) connected to the gate (G). The channel is depleted by applying a negative voltage on the gate.

(b) The graph illustrates the relationship between the drain current ($I_D$) and the gate-source voltage ($V_{GS}$) for a p-channel depletion-type MOSFET. The drain current decreases as the gate-source voltage increases.

(c) The family of curves shows the change in the drain current for different gate-source voltages ($V_{GS}$). The curves illustrate the saturation region where the drain current becomes independent of the gate-source voltage.
The Field Effect Transistor

Enhancement-type MOSFET

The structure of the enhancement-type MOSFET has no built-in channel. Its operation is quite unique and transfer characteristics are not defined by Shockley equation.
The Field Effect Transistor

Operation and Characteristics of Enhancement-type MOSFET

When \( V_{GS} = 0, I_D = 0 \). However, when \( V_{GS} \) is positive, the gate attracts electrons from the substrate which forms into an n-channel. \( V_{GS} \) may be increased until a measurable flow of electrons occurs between source and drain. The value of \( V_{GS} \) which causes measurable current to flow is called the threshold voltage, \( V_T \). Further increases in \( V_{GS} \) will result in pinch-off.
The Field Effect Transistor

Notice the increase in separation

\[ V_{DS_{sat}} = V_{GS} - V_T \]

The "k" term is a constant that is a function of the construction of the device. It may be determined from

\[ I_D = k(V_{GS} - V_T)^2 \]

The "k" term is a constant that is a function of the construction of the device. It may be determined from

\[ k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \]

\[ I_{Don} \text{ and } V_{GSon} \text{ may be determined from the curve} \]
The Field Effect Transistor

p-Channel Enhancement-type MOSFET
The Field Effect Transistor

Complementary MOSFETs (CMOS)

When p-channel and n-channel MOSFETs are constructed on the same substrate, very effective logic circuits may be created. This configuration consumes very little power, have very fast switching speeds, has very high input impedance.
The Field Effect Transistor

MESFET

The basic structure of a MESFET is shown below:

The Gate is connected directly to the metal barrier called Schottky barrier. These type of barriers are made by depositing a metal such as tungsten directly on an n-type channel. This is unlike the MOSFETs which are connected to an insulating layer instead.
### TABLE 6.2

<table>
<thead>
<tr>
<th>Type</th>
<th>Symbol and Basic Relationships</th>
<th>Transfer Curve</th>
<th>Input Resistance and Capacitance</th>
</tr>
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<tbody>
<tr>
<td>JFET (n-channel)</td>
<td>$I_D = \frac{V_D}{R_D}$</td>
<td>$I_D$</td>
<td>$R_D &gt; 10^6 \Omega$</td>
</tr>
<tr>
<td></td>
<td>$I_{DS} = \frac{V_{DS}}{R_{DS}}$</td>
<td></td>
<td>$C_D \approx 1 - 10 \text{ pF}$</td>
</tr>
<tr>
<td>MOSFET depletion type (n-channel)</td>
<td>$I_D = \frac{V_D}{R_D}$</td>
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The Field Effect Transistor

A more Advanced Look at the n-channel MOS (enhancement type): NMOS

These are some of the basis of IC designs. W/L is important in Scaling transistor sizes. Latest Technology has L = 45 nm