Trends and challenges in VLSI at Device level: Carbon Electronics

Anurag Srivastava
Content

• History of VLSI
• Moore’s Law
• Conventional devices
• Challenges in conventional devices
• New Technologies(Beyond Si)
• Conclusion
History of VLSI

- With the invention of transistors at Bell Labs in 1947, the field of electronics shifted from vacuum tubes to solid-state devices.
- Late 50s First IC (JK-FF by Jack Kilby at TI)

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology</th>
<th>No. of transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Early 50’s</td>
<td>SSI</td>
<td>10</td>
</tr>
<tr>
<td>Late 60’s</td>
<td>MSI</td>
<td>100</td>
</tr>
<tr>
<td>Early 70’s</td>
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<td>1000</td>
</tr>
<tr>
<td>Early 80’s</td>
<td>VLSI</td>
<td>10000</td>
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</table>
Moore’s Law
Scaling

Focus of this talk: emerging nanoelectronic devices

Note: Future options subject to change
Conventional semiconductor devices

- Diode
- Transistor
  - BJT
  - FET
  - JFET
  - MOSFET - “most used semiconductor device today”
MOSFET (Regions of Operation)

- **Source** \( V_{GS} < V_{TH} \) to **Drain**
  - **P+** \( \text{P substrate} \)
  - **N+** \( \text{depletion region} \)

- **Source** \( V_{GS} \geq V_{TH} \) to **Drain**
  - **P+** \( \text{P substrate} \)
  - **N+** \( \text{depletion region} \)

- **Linear operating region (ohmic mode)**
  - **Source** \( V_{DS} < V_{GS} - V_{TH} \) to **Drain**
  - **P+** \( \text{P substrate} \)
  - **N+** \( \text{depletion region} \)

- **Saturation mode at point of pinch-off**
  - **Source** \( V_{GS} \geq V_{TH} \) to **Drain**
  - **P+** \( \text{P substrate} \)
  - **N+** \( \text{pinched-off channel} \)

- **Saturation mode**
  - **Source** \( V_{GS} \geq V_{TH} \) to **Drain**
  - **P+** \( \text{P substrate} \)
  - **N+**
The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices.

The MOSFET is a four terminal device with source (S), gate (G), drain (D) and body (B) terminals. The body of the MOSFET is frequently connected to the source terminal so making it a three terminal device like field effect transistor. The MOSFET is very far the most common transistor and can be used in both analog and digital circuits.
The MOSFET works by electronically varying the width of a channel along which charge carriers flow (electrons or holes). The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide. The MOS capacity present in the device is the main part
The MOSFET can function in two ways
Depletion Mode
Enhancement Mode

**Depletion Mode:**
When there is no voltage on the gate, the channel shows its maximum conductance. As the voltage on the gate is either positive or negative, the channel conductivity decreases. For example
The MOSFET can function in two ways

Depletion Mode

Enhancement Mode

Enhancement mode:
When there is no voltage on the gate the device does not conduct. More is the voltage on the gate, the better the device can conduct.
Working Principle of MOSFET:

The aim of the MOSFET is to be able to control the voltage and current flow between the source and drain. It works almost as a switch. The working of MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer which is located between source and drain terminal. It can be inverted from p-type to n-type by applying a positive or negative gate voltages respectively. When we apply the positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward with the substrate. The depletion region populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage, a hole channel will be formed under the oxide layer.
Mechanisms that contribute to total leakage power in nano-scale MOS devices. [2]

I1 : Reverse bias pn junction leakage
I2: Sub threshold leakage
I3: Oxide tunneling current
I4: Gate current due to hot carrier injection
I5 : GIDL
I6 : Channel punchthrough
Effects of device scaling

As the device scaling is approaching its physical size limitations, the technology cycle is getting slow down due to

- Increasing power consumption
- Loss of Mobility
- Difficulty on increase of on-current
- process variation
- Increased fabrication cost
- low reliability and yield
Challenges in conventional devices

- As the size becomes further smaller, scaling the silicon MOSFET becomes harder.
- Faces serious limitation in fabrication technology.
- Device performance degradation.
- Requirement of high performance channel material.
- Mobility enhancement technology requirement.
“Beyond CMOS”

More Moore >> “End of traditional scaling

More than Moore: MEMS, RF, HV, sensing

Beyond CMOS
New Technologies

• With the end of Si FET scaling appearing increasingly near, searching for more scalable transistor structures in Si and in “beyond-Si” solutions has become imperative; from relatively “easy” transitions to non-planar Si structures, to the incorporation of high mobility semiconductors, like Ge and III-V’s, to even higher mobility new materials such as carbon nanotubes, graphene, or other molecular structures. [1]
According to the statistics provided by the International Technology Roadmap for Semiconductors, some of the emerging devices which have the potential to replace Si in the non-si era are:-

- Nanowire Field-Effect Transistor (NW-FETs).
- Compound Semiconductor FET.
- Graphene NanoRibbon Transistor.
- Carbon Nanotube Based Field Effect Transistor (CNTFET).
Nanowire Field-Effect Transistor

Advantages: 1-D conduction, reduction of scattering, minimized short channel effects.

Disadvantages: use of metal source-drain junctions, results in ambipolar conduction, variation in nanowire due to fabrication imperfection leads to perturbation in carrier potential.
Compound Semiconductor FET

- **Advantages:** Can deliver 3 times higher performance than silicon and can deliver the same performance as obtained by MOSFET at one-tenth power consumption of silicon.
- **Disadvantages:** Can cause excessive leakage and large static power dissipation. The difficulties of forming a high k-dielectric for better electrostatic control of the device.
Graphene NanoRibbon Transistor

• Advantages: Using Graphene as a channel material, due to high mobility of graphene, it will result in fast switching, monolayer thin body for optimum electrostatic scaling and excellent thermal conductivity.

• Disadvantages: Low Ion/Ioff (a measure of how much power is consumed by the circuit when it is in standby mode) i.e. if Ion/Ioff is low, the IC made of billions of graphene transistor will consume as enormous amount of energy.
Carbon Nanotube Based Field Effect Transistor

- Superior material properties, such as large current carrying capacity, the excellent mechanical and thermal stability, and high thermal conductivity.
- NMOS and PMOS transistors show almost identical I-V characteristics, it becomes a significant advantage for CMOS circuit design.
Furthermore, they are very attractive to Si-based semiconductor industry for the following reasons:

1) CNTFETs show considerable improvement in device performance metrics such as low power and high speed.

2) Their operating principles and devices structure are similar to Si-based CMOS transistors; therefore, the CMOS design infrastructure could be reused.
Conclusion

• Nanoelectronics research is the main enabler & driver of all current & future applications with demanding requirements (low cost/power, high frequencies etc).

• Various new nanoelectronic devices, so called “Beyond CMOS Devices,” are actively being investigated and researched to supplement or possibly replace ultimately scaled conventional CMOS devices.

• While those nanoelectronic devices offer ultra-high density system integration, they are still in a premature stage having many critical issues such as high variations and deteriorated reliability. The practical realization of those promising technologies requires extensive researches from device to system architecture level.

2. Leakage current mechanism and leakage reduction techniques in deep submicrometer cmos circuits, Kaushik Roy et al., proceedings of IEEE, Vol 91, No. 2, February 2003

3. Carbon nano tube field effect transistor: A review, PA ALVI et al., Indian journal of pure & applied physics, vol.43, Dec 2005, pp. 899-904

Carbon -Electronics

Anurag Srivastava
Contents

- Setbacks of MOSFETs
- Introduction to CNTFETs
- CNTFET working
- Important aspects of CNTFET
- Effect of diameter variation
- Conclusion
- Future Work
Setbacks of MOSFETs

• A MOSFET is a
  • Semiconductor device,
  • most commonly used in the field of VLSI Design, and Power electronics.

• The scaling of MOSFET has been the driving force towards the technological advancement, But Continuous scaling include
  
  – short channel effects (In electronics, short-channel effects occur in MOSFETs in which the channel length is comparable to the depletion layer widths of the source and drain junctions. These effects include, in particular, drain-induced barrier lowering, velocity saturation, and hot carrier degradation.)
  
  – high leakage current (leakage current is defined as the current that "leaks" between drain and source (D/S) of a MOSFET when the device is OFF, i.e, its Vgs is below the device threshold voltage. In most case, when the leakage is mentioned, it is referring to Id current.)
  
  – excessive process variation (Process variation is the naturally occurring variation in the attributes of transistors (length, widths, oxide thickness) when integrated circuits are fabricated. The amount of process variation becomes particularly pronounced at smaller process nodes (<65 nm) as the variation becomes a larger percentage of the full length or width of the device and as feature sizes approach the fundamental dimensions such as the size of atoms and the wavelength of usable light for patterning lithography masks.)
  
  – reliability issues (Negative Bias-Temperature Instability (NBTI), Positive Bias-Temperature Instability (PBTI) and Hot-Carrier Degradation (Occurs with NBTI/PBTI when non-zero voltage is applied at the drain))
Impact of nanotechnology with time

Focus of this talk: emerging nanoelectronic devices

Note: Future options subject to change
Why CNTFET?

- As the size becomes smaller, scaling the silicon MOSFET becomes harder.
- Requirement of high performance channel material.
- Mobility enhancement technology requirement.

Advantage of using CNTFET

✓ 1-D ballistic transport of electrons and holes.

✓ High drive current (For bipolar transistors, a large base current is required to maintain low on-voltage. However, since the MOSFET is a voltage control element, it can drive with small power sufficient to charge the gate. But because the input capacitance (Ciss) of the power MOSFET is rather large for high-speed switching, it is necessary to quickly charge the input capacitance with a low-impedance drive circuit.) and large transconductance (for transfer conductance), also infrequently called mutual conductance, is the electrical characteristic relating the current through the output of a device to the voltage across the input of a device. Conductance is the reciprocal of resistance.).

✓ High temperature resilience and strong covalent bond (Large Si atom in comparison to carbon).
Why CNTFET?

• According to Moore's law, the dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years.
• This scaling down of devices has been the driving force in technological advances since the late 20th century. However, as noted by ITRS 2009 edition, further scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range.
• The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping.
• These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk MOSFET structure with a single carbon nanotube or an array of carbon nanotubes.
CNT: The ideal transistor Material

- Carbon nanotubes (CNTs) were discovered by Ijima in Japan in 1991.
- CNTs can be thought as rolled up sheets of graphene.
- Electrical properties depend on chirality or the direction of this distortion.
- CNTs can be metallic or semiconducting depending on the chirality.

Fig.1: Strip of graphene sheet rolled up into tube
Electronic structure of carbon nanotubes

The exceptional electrical properties of carbon nanotubes arise from the unique electronic structure of graphene itself that can roll up and form a hollow cylinder. The circumference of such carbon nanotube can be expressed in terms of a chiral vector: \( \hat{C}_h = n\hat{a}_1 + m\hat{a}_2 \) which connects two crystallographically equivalent sites of the two-dimensional graphene sheet. Here \( n \) and \( m \) are integers and \( \hat{a}_1 \) and \( \hat{a}_2 \) are the unit vectors of the hexagonal honeycomb lattice. Therefore, the structure of any carbon nanotube can be described by an index with a pair of integers \((n,m)\) that define its chiral vector.

\[
C = na_1 + ma_2
\]

\( n, m \) = chirality parameter

\( a_1 = a (\sqrt{3}, 0) \)

\( a_2 = a \left( \frac{\sqrt{3}}{2}, \frac{\sqrt{3}}{2} \right) \)

Where \( a = 0.142 \) Å bond length between two carbon atoms.

If \( n=m \) structure is armchair

If \( n \) or \( m=0 \) structure is zigzag

Nanotube diameter and chiral angles are given as

\[
d_t = \frac{\sqrt{3}a_{c-c}\sqrt{m^2+mn+n^2}}{\pi} \quad \theta = \tan^{-1} \frac{\sqrt{3}n}{2m+n}
\]
CNTFET Type

- **Based on geometry**
  - Top Gate
  - Bottom Gate
  - Coaxial Gate

- **Based on operation**
  - Schottky barrier
  - MOSFET like
  - T-CNTFET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
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<tr>
<td>$L_{ch}$</td>
<td>Physical channel length</td>
<td>32 nm</td>
</tr>
<tr>
<td>$L_{geff}$</td>
<td>The mean free path in the intrinsic CNT channel</td>
<td>100 nm</td>
</tr>
<tr>
<td>$L_{dd}$</td>
<td>The length of doped CNT drain-side extension region</td>
<td>32 nm</td>
</tr>
<tr>
<td>$L_{ss}$</td>
<td>The length of doped CNT source-side extension region</td>
<td>32 nm</td>
</tr>
<tr>
<td>$T_{ox}$</td>
<td>The thickness of high-k top gate dielectric material</td>
<td>4 nm</td>
</tr>
<tr>
<td>$K_{gate}$</td>
<td>The dielectric constant of high-k top gate dielectric material</td>
<td>16</td>
</tr>
<tr>
<td>$E_{Fi}$</td>
<td>The Fermi level of the doped S/D tube</td>
<td>6 eV</td>
</tr>
<tr>
<td>$C_{sub}$</td>
<td>The coupling capacitance between the channel region and the substrate</td>
<td>20 pF/m</td>
</tr>
</tbody>
</table>
Bottom gate CNTFET

- The first CNTFET was fabricated in 1998. These were simple devices fabricated by depositing single-wall CNTs (synthesized by laser ablation) from solution onto oxidized Si wafers which had been prepatterned with gold or platinum electrodes.
- The devices displayed high on-state resistance of several MQ, low transconductance (-1,\(\sim\)) and no current saturation, and they required high gate voltages (several volts) to turn them on.
Top gate CNTFET

- The next generation of CNTFET came in top-gated structure to improve the device performance.
- This structure gives better out-turn than early structure. The improvement comes from the scaling of the dimension and the adoption of better device geometry as well as the device performance.
Coaxial gate CNTFET

• Gate all around geometry.
• More electrostatic control over channel.
Working principle

• Basic principle operation of CNTFET is the same as MOSFET where electrons are supplied by source terminal and drain terminal will collect these electrons.
• In other words, current is actually flowing from drain to source terminal.
• Gate terminal controls current intensity in the transistor channel and the transistor is in off state if no gate voltage is applied.
SB-CNTFET

- SB-CNFET works on the principle of direct tunneling through the Schottky barrier at the source channel junction.
- The barrier width is controlled by the gate voltage and hence the transconductance of the device depends on the gate voltage.
- At low gate bias, large barrier limits the current in the channel. As gate bias is increased, it reduces the barrier width, which increases quantum mechanical tunneling through the barrier, and therefore increases current flow in transistor channel.
- In SBCNFET, the transistor action occurs by modulating the transmission coefficient of the device.

![Diagram of SBCNTFET](image)
MOSFET like CNTFET

• The structure of this device is slightly different than SB-CNFET since it used heavily doped terminals instead of metal.
• This device is formed in order to overcome problems in SB-CNFET by operating like normal MOSFET.
• This device operates on the principle of modulation the barrier height by gate voltage application. The drain current is controlled by number of charge that is induced in the channel by gate terminal.

![Diagram of MOSFET like CNTFET](image-url)
How CNTFET works?

- Operation of CNTFET compared with Si-MOSFET
Continued....

Standard MOSFET

\[ I_d = \frac{W}{L} \mu_{eff} C_{ox} (V_g - V_t) V_{ds} \]

- carrier mobility
- spatial dependence
- charge in channel
- bias dependence

\[ \rightarrow \text{no DOS consideration} \]
\[ \rightarrow \text{no consideration of contacts} \]

CNTFET

\[ I_d = q \int_{E_{fs}}^{E_{fd}} f(E,T) \cdot v(E) \cdot T(E) \cdot D(E) \cdot dE \]

- charge in channel
- transmission at contacts
- bias dependence (carrier injection determined by states between source/drain Fermi levels)

\[ \rightarrow \text{no spatial dependence} \]
\[ \rightarrow \text{no mobility dependence} \]
Id/Vds curve
EDP of CNTFET and MOSFET (45nm Process)

- MOSFET ($t_{\text{node}} = 45$ nm)
- CNTFET ($L_{\text{wire}} = 5 \mu m, t_{\text{sub}} = 500$ nm)
- CNTFET ($L_{\text{wire}} = 1 \mu m, t_{\text{sub}} = 500$ nm)
- CNTFET ($L_{\text{wire}} = 0 \mu m, t_{\text{sub}} = 500$ nm)

Energy Delay Product (J.s)

Logic Gates:
- INV
- NAND2
- NAND3
- NOR2
- NOR3

Graph shows the Energy Delay Product for different logic gates and CNTFET configurations compared to MOSFET.
<table>
<thead>
<tr>
<th></th>
<th>MOSFET</th>
<th>CNTFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gc</td>
<td>5uF/cm²</td>
<td>2.4uF/cm²</td>
</tr>
<tr>
<td>Id</td>
<td>500uA/µm</td>
<td>1500 uA/µm</td>
</tr>
<tr>
<td>Mobility</td>
<td>7x10^6 cm/s</td>
<td>3.5x10^6 cm/s</td>
</tr>
<tr>
<td>Thermal velocity</td>
<td>-</td>
<td>2 times of mosfet</td>
</tr>
</tbody>
</table>
Important aspects of CNTFETs

• Main aspects which impacts on operation and performance of CNTFET
  ➢ Contact
  ➢ Dielectric
  ➢ Gate structure
  ➢ Passivation Treatment
Contacts

• Schottky barrier height depends on metal contact work function.

• Adhesion between metal and CNT also important since a tunneling barrier forms that limits the current.

![Diagram of CNTFET device with pd contacts](image)

Fig. : CNTFET device with pd contacts, On current for different contact metals

Dielectric

- Choosing a dielectric for CNTFETs is not related to Fermi level pinning or passivating surface states.
- The most common fabrication method for depositing high quality high-\(\kappa\) dielectrics is atomic layer deposition (ALD).

Fig. : On current for different dielectric constant values (a. simulated results b. experimental) Guo, Jing et al.(2004)
Conti....

- High-k dielectric materials can provide efficient charge injection to channel.
- Reduces direct tunneling.
- Provides high gate capacitance.

Fig. : CNTFET parasitic model with intrinsic and extrinsic capacitance.
Gate capacitance

\[ C_{ox} = 2\pi \varepsilon \frac{L_g}{\ln\left(\frac{t_{ox} + r_{cnt}}{r_{cnt}}\right)} \]

- \( t_{ox} = \text{Gate dielectric thickness} \)
- \( \varepsilon = \text{Dielectric constant of gate insulator} \)
- \( L_g = \text{Gate length} \)
- \( r_{cnt} = \text{nanotube diameter} \)

\[ C_q = \frac{\partial Q}{\partial V_S} \]

- \( \partial Q = \text{Charge on channel} \)
- \( \partial V_S = \text{Channel potential} \)

Fig. : Gate capacitance with dielectric constant
Zoheir Kordrostami and Mohammad Hossein Sheikh (2010)
Gate structure

- CNTFETs are not substrate bound.
- Freedom in designing gate structure.

![Diagram showing different gate geometries of CNTFETs](image)

- Top Gate
- Bottom Gate
- Wrap around gate

Fig. : Different gate geometries of CNTFET
Passivation Treatment

• Any adsorbate is readily detected by conductance changes in a CNT.
• Nanotube sensitivity to such stray charges is a challenge for high performance digital applications.
• Large variation of threshold voltage (Vt) among CNTFETs of the same geometry and the sizable hysteresis.
• The simple application of a hydrophobic self-assembled monolayer in vacuum to passivate (cover) the exposed CNT channel and surrounding dielectric surface is able to reduce the range of Vt by more than 50%.
Effect of diameter variation on CNTFET

- We have studied the model of coaxial CNTFET.
- Analysed the diameter variation effects on device characteristics.
Modelling of the *CNTFET device*

- The simulations perform a self-consistent solution between Poisson’s equation and the nonequilibrium Green’s function (NEGF) equations.
- A two-dimensional Poisson equation is solved in the cylindrical coordinates for coaxially gated CNTFETs. The permittivity varies only in the radial direction.
- For the Schottky-barrier CNTFETs, Dirichlet boundary conditions are used at the source, drain, and gate.
- Von Neumann boundary conditions are used along the exposed surface of the dielectric. There, the radial component of the electric field is set to zero.
• A zero field boundary condition is applied at the source and drain ends for the CNTFETs with doped reservoirs. There, the axial component of the electric field is set to zero.

• The CNT is modeled using a tight binding -bond model with one orbital per carbon atom.

• The Hamiltonian matrix elements are taken from [48].

• The recursive Green function algorithm is used to solve the NEGF equations for the mean field charge density and current. The surface Green’s function is calculated using decimation method [42], [49], [50]
Specification of the device

- Channel length: **14nm**
- gate insulator thickness: **1.5e-09 (m)**
- insulator dielectric constant: **3.9**
- temperature: **300 (K)**
- initial gate voltage: **0 (eV)**
- final gate voltage: **1 (eV)**
- number of bias points (gate): **13**
- initial drain voltage: **0 (eV)**
- final drain voltage: **1 (eV)**
- number of bias points (drain): **13**
- threshold voltage: **0.32**
Dependence of diameter of CNT on the characteristics of CNTFET

• Drain Current vs Gate Voltages
• Drain Current vs Drain Voltages
• Quantum Capacitance vs Gate Voltage
• Ratio of Transconductance and Drain current vs Gate Voltage
• Other parameters with respect to diameter variations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$I_{On}(A)$</th>
<th>Leakage current (A)</th>
<th>(DIBL (mV/V))</th>
<th>Voltage gain ($A_V$)</th>
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<td>6.798e-05</td>
<td>6.611e-11</td>
<td>5.28</td>
<td>25.13</td>
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Summary

- CNTFET has capability to use as a future nanoscale transistor.
- All the aspects which are important in performance analysis of CNTFET are discussed.
- Increasing cnt diameter has good effect on cntfet as seen from results.
References


